CLAIMS

1. (Currently amended) A bias circuit comprising:

a reference cell to generate a bias signal; and

a first component coupled to the reference cell to adjust the bias signal by replicating a thermal characteristic of a second component that may be coupled to the bias circuit;

wherein the reference cell includes a ~~feedback loop to drive a pair of ΔV_{BE} transistors~~ first junction to operate at a first current density, a second junction coupled to the first junction to operate at a second current density that is substantially different than the first current density, and a first resistor coupled to the first junction at a summing node; and

wherein the first component is ~~arranged in the feedback loop~~ coupled to the summing node.

2. (Canceled)

3. (Currently amended) A bias circuit according to claim 1 ~~wherein the feedback loop comprises~~ further comprising a current mirror coupled between the first component and the reference cell in a feedback loop arrangement.

4. (Original) A bias circuit according to claim 3 wherein the current mirror is arranged to load the reference cell.

5. (Original) A bias circuit according to claim 1 wherein the first component comprises a transistor.

6. (Canceled)

7. (Currently amended) A bias circuit according to claim 1 wherein the ~~reference cell and the first component are coupled together at a summing node~~ first component is coupled to the summing node through a second resistor.

8. (Original) A bias circuit according to claim 1 further comprising a clamping circuit coupled to the reference cell.

9. (Currently amended) A method comprising:

generating a bias signal ~~with a reference cell having a feedback loop to drive a pair of ΔV_{BE} transistors;~~ by operating a bandgap cell to generate a PTAT current in a first resistor;

generating a compensation current by operating a replica component under similar operating conditions to a component that may be coupled to the bias circuit;

adjusting the bias signal by ~~replicating a thermal characteristic of a component that may be coupled to the bias circuit by operating a replica component in the feedback loop~~ coupling the compensation current to the first resistor, thereby summing the PTAT current and the compensation current.

10. (Currently amended) A method according to claim 9 wherein ~~replicating the thermal characteristic comprises operating a replica component under similar operating conditions to the component that may be coupled to the bias circuit~~ the replica component is operated in a feedback loop with the bandgap cell.

11. (Canceled)

12. (Currently amended) A method according to claim [[9]] 10 wherein operating [[a]] the replica component in [[a]] the feedback loop comprises mirroring current through the replica component into the ~~reference~~ bandgap cell.

13. (Currently amended) A method according to claim 9 wherein ~~adjusting the bias signal comprises summing a current from a replica component with a current from the reference cell~~ the compensation current is coupled to the first resistor through a second resistor.

14. (Currently amended) A method according to claim 9 further comprising clamping a voltage of the ~~reference~~ bandgap cell.

15. (Currently amended) A system comprising:

a first circuit comprising a reference cell to generate a bias signal, and a first component coupled to the reference cell; and

a second circuit coupled to the first circuit to receive the bias signal, the second circuit comprising a second component;

wherein the first component is arranged to adjust the bias signal by replicating a thermal characteristic of the second component;

wherein the reference cell includes a ~~feedback loop to drive a pair of ΔV_{BE} transistors~~ first junction to operate at a first current density, a second junction coupled to the first junction to operate at a second current density that is substantially different than the first current density, and a first resistor coupled to the first junction at a summing node; and

wherein the first component is ~~arranged in the feedback loop~~ coupled to the summing node.

16. (Canceled)

17. (Currently amended) A system according to claim 15 ~~wherein the feedback loop comprises~~ further comprising a current mirror coupled between the first component and the reference cell in a feedback loop arrangement.

18. (Currently amended) A system according to claim 15 wherein the ~~reference cell and the first component are coupled together at a summing node~~ first component is coupled to the summing node through a second resistor.

19. (Original) A system according to claim 15 wherein the first and second components have a matching thermal characteristic.

20. (Currently amended) A bias circuit comprising:

bias means for generating a bias signal~~, wherein the bias means comprises a feedback loop arranged to drive a pair of ΔVBE transistors~~ by operating a bandgap cell to generate a PTAT current in a first resistor; and

replication means for ~~replicating a thermal characteristic of a component that may be coupled to the bias circuit, wherein the replication means comprises a replication component that is matched to the component that may be coupled to the bias circuit~~ generating a compensation current by operating a replica component under similar operating conditions to a component that may be coupled to the bias circuit;

wherein the ~~replication component is arranged in the feedback loop~~ compensation current is coupled to the first resistor, thereby summing the PTAT current and the compensation current.

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Currently amended) A bias circuit according to claim 20 further comprising means for controlling the amount of compensation provided by the replication means.

25. (New) A bias circuit according to claim 1 further comprising a third resistor coupled between the second junction and the first resistor at a common node.